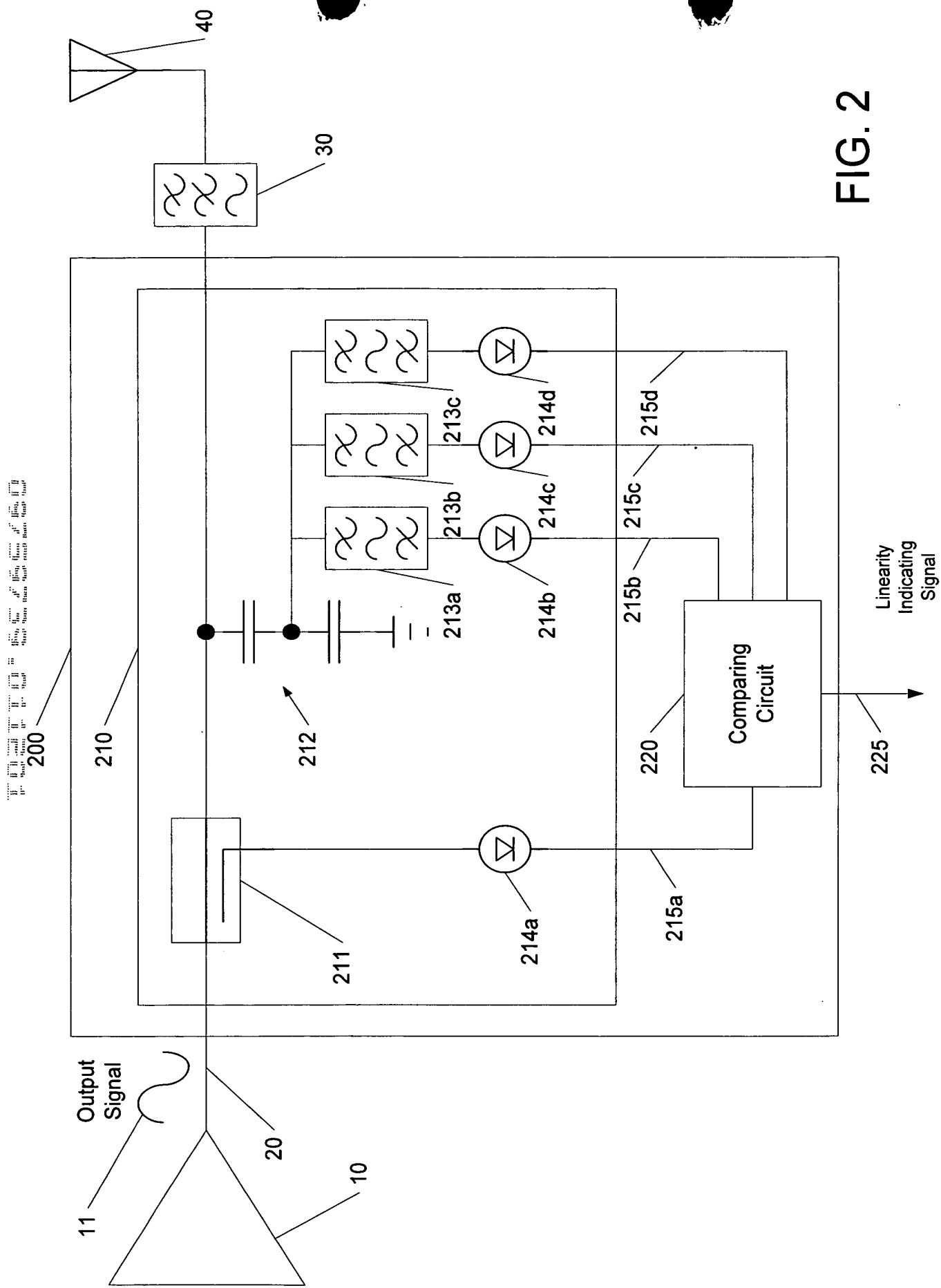


FIG. 1



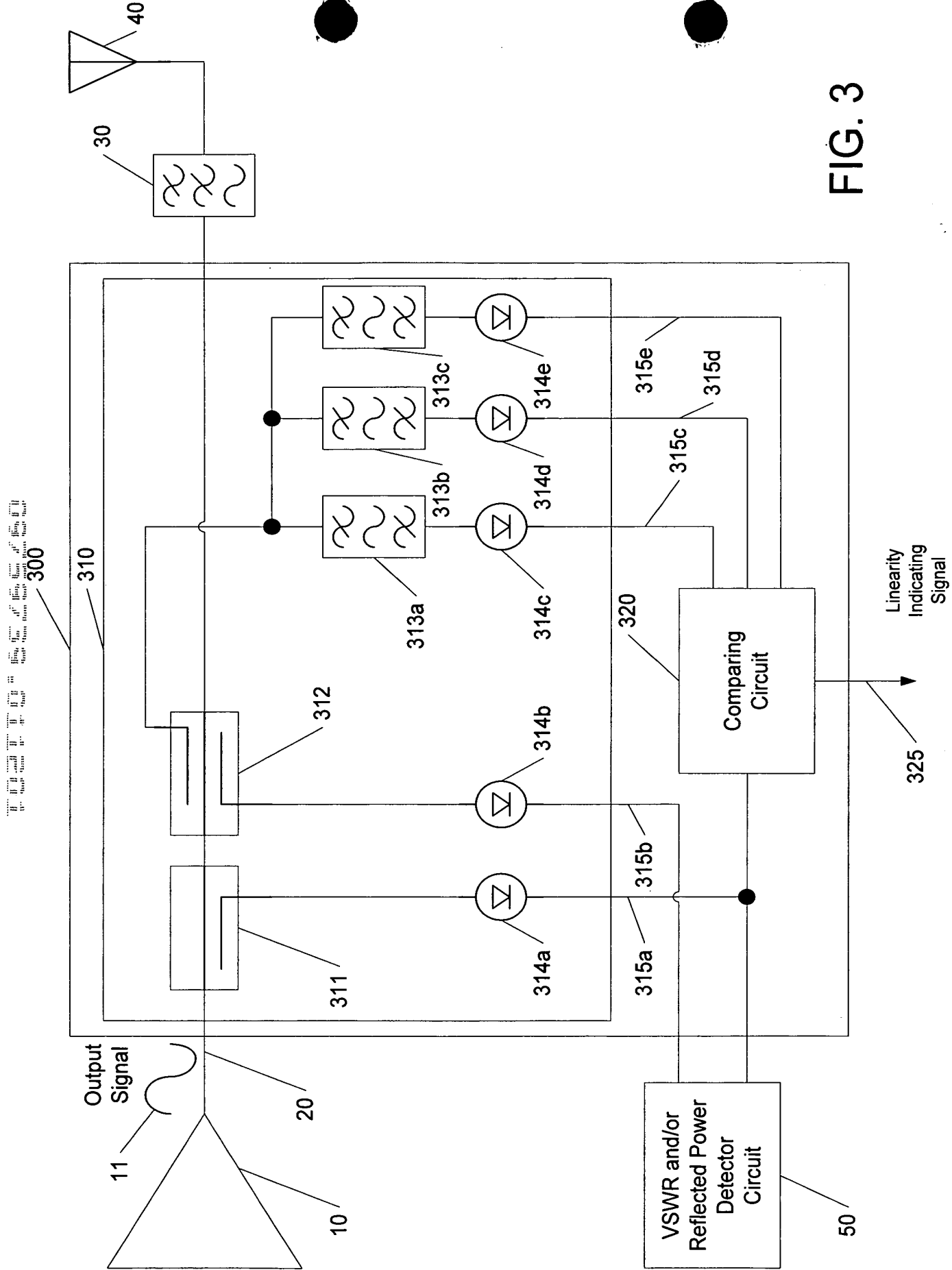


FIG. 4 is a block diagram of a system for measuring the linearity of a device under test (DUT) 10. The system includes an input signal source 20, a DUT 10, an output signal source 11, a VSWR and/or Reflected Power Detector Circuit 50, a Comparing Circuit 420, and a Linearity Indicating Signal output 425. The DUT 10 is connected to the input signal source 20 and the output signal source 11. The output signal source 11 is connected to the VSWR and/or Reflected Power Detector Circuit 50. The VSWR and/or Reflected Power Detector Circuit 50 is connected to the Comparing Circuit 420. The Comparing Circuit 420 is connected to the Linearity Indicating Signal output 425. The system also includes a feedback loop 400 that includes a feedback signal source 30 and a feedback signal output 40. The feedback signal source 30 is connected to the feedback signal output 40, which is connected to the input signal source 20. The feedback signal output 40 is also connected to the VSWR and/or Reflected Power Detector Circuit 50. The VSWR and/or Reflected Power Detector Circuit 50 is connected to the Comparing Circuit 420. The Comparing Circuit 420 is connected to the Linearity Indicating Signal output 425. The system also includes a feedback loop 400 that includes a feedback signal source 30 and a feedback signal output 40. The feedback signal source 30 is connected to the feedback signal output 40, which is connected to the input signal source 20. The feedback signal output 40 is also connected to the VSWR and/or Reflected Power Detector Circuit 50. The VSWR and/or Reflected Power Detector Circuit 50 is connected to the Comparing Circuit 420. The Comparing Circuit 420 is connected to the Linearity Indicating Signal output 425.

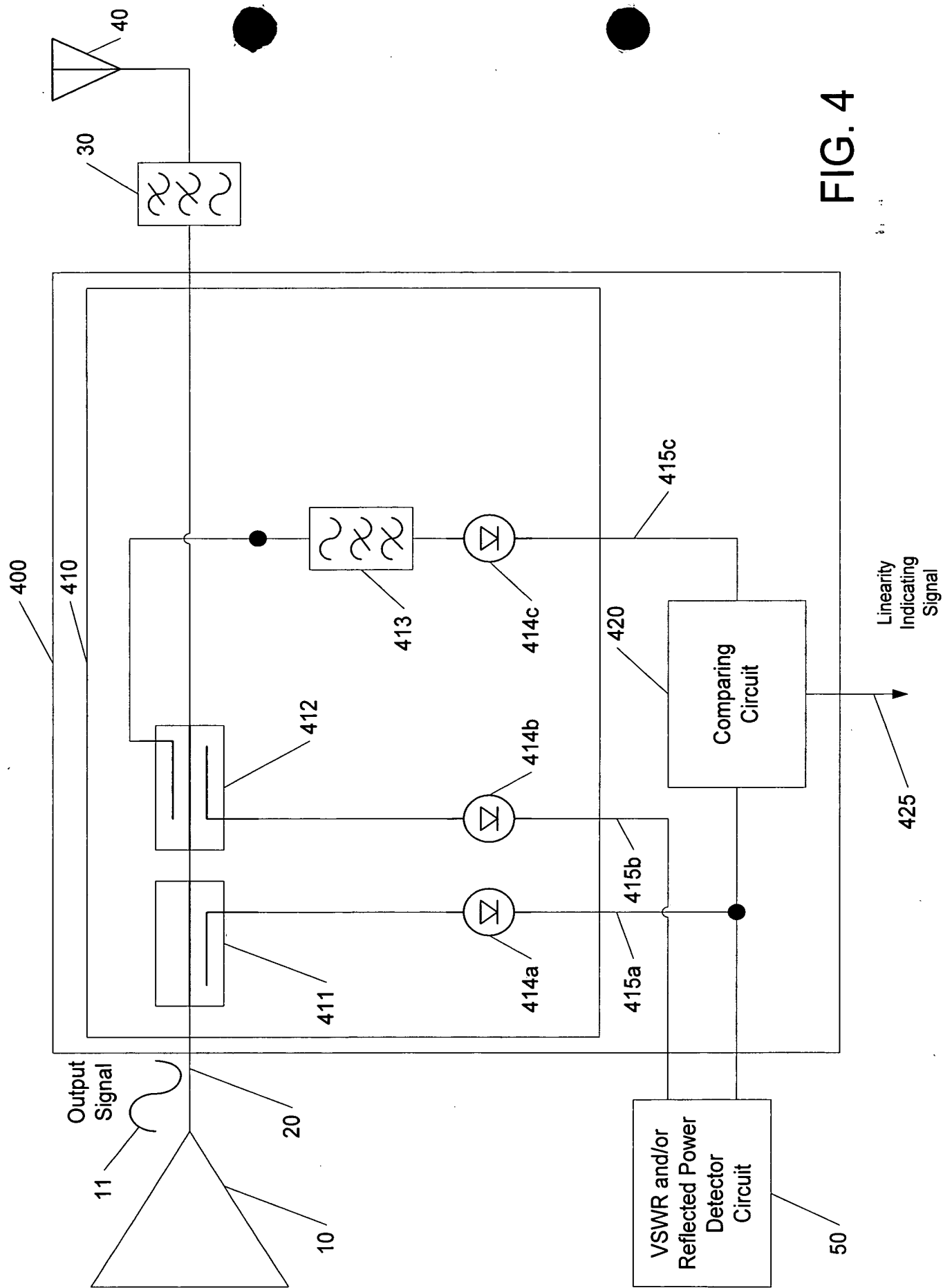


FIG. 4

FIG. 5 is a block diagram of a system 10 for processing an input signal. The system 10 includes an input signal 11, a filter 20, a detector 520, a control circuit 530, and an output signal 510. The input signal 11 is received by the filter 20, which outputs a signal to the detector 520. The detector 520 outputs a signal to the control circuit 530, which outputs a signal to the output signal 510.

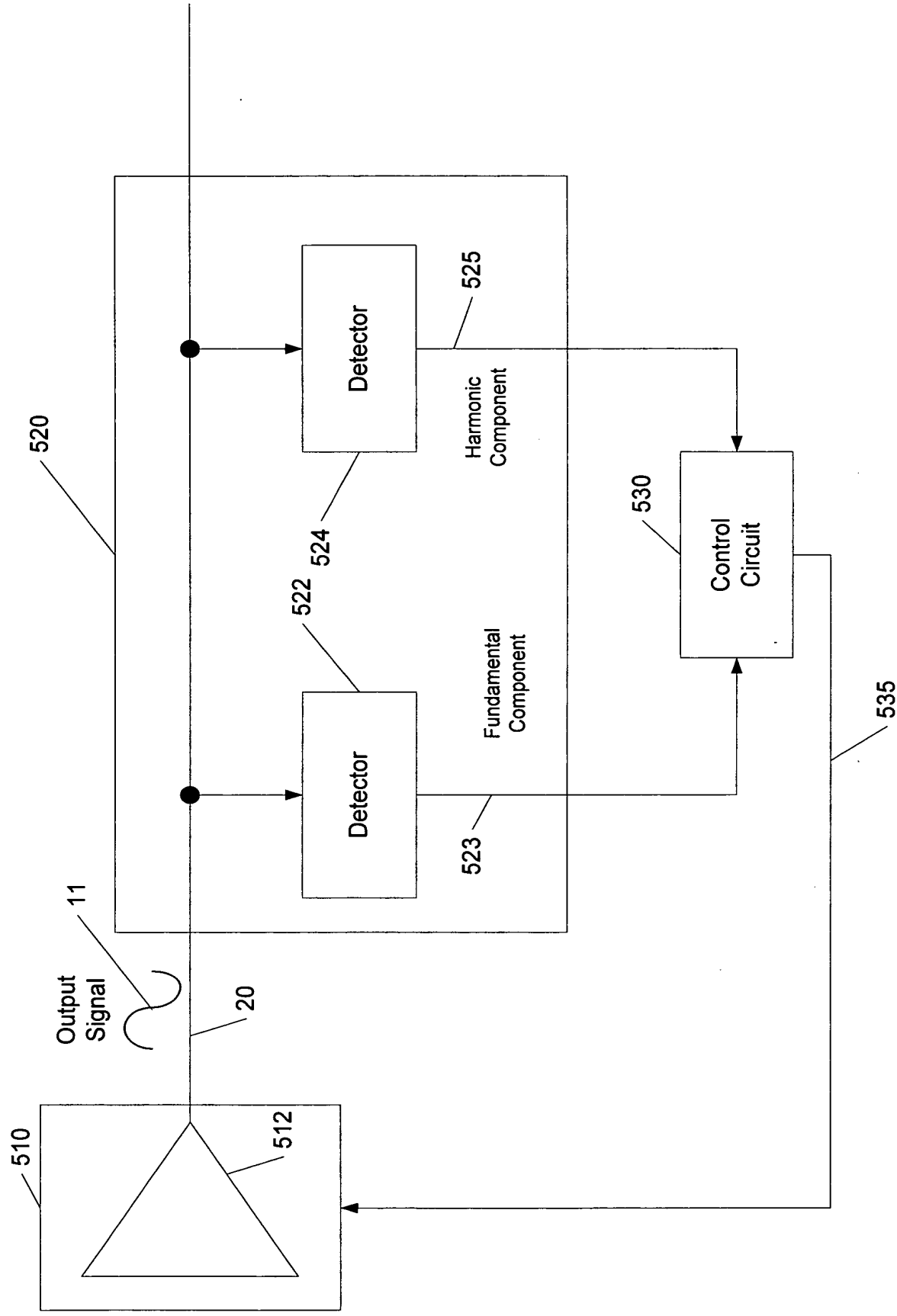
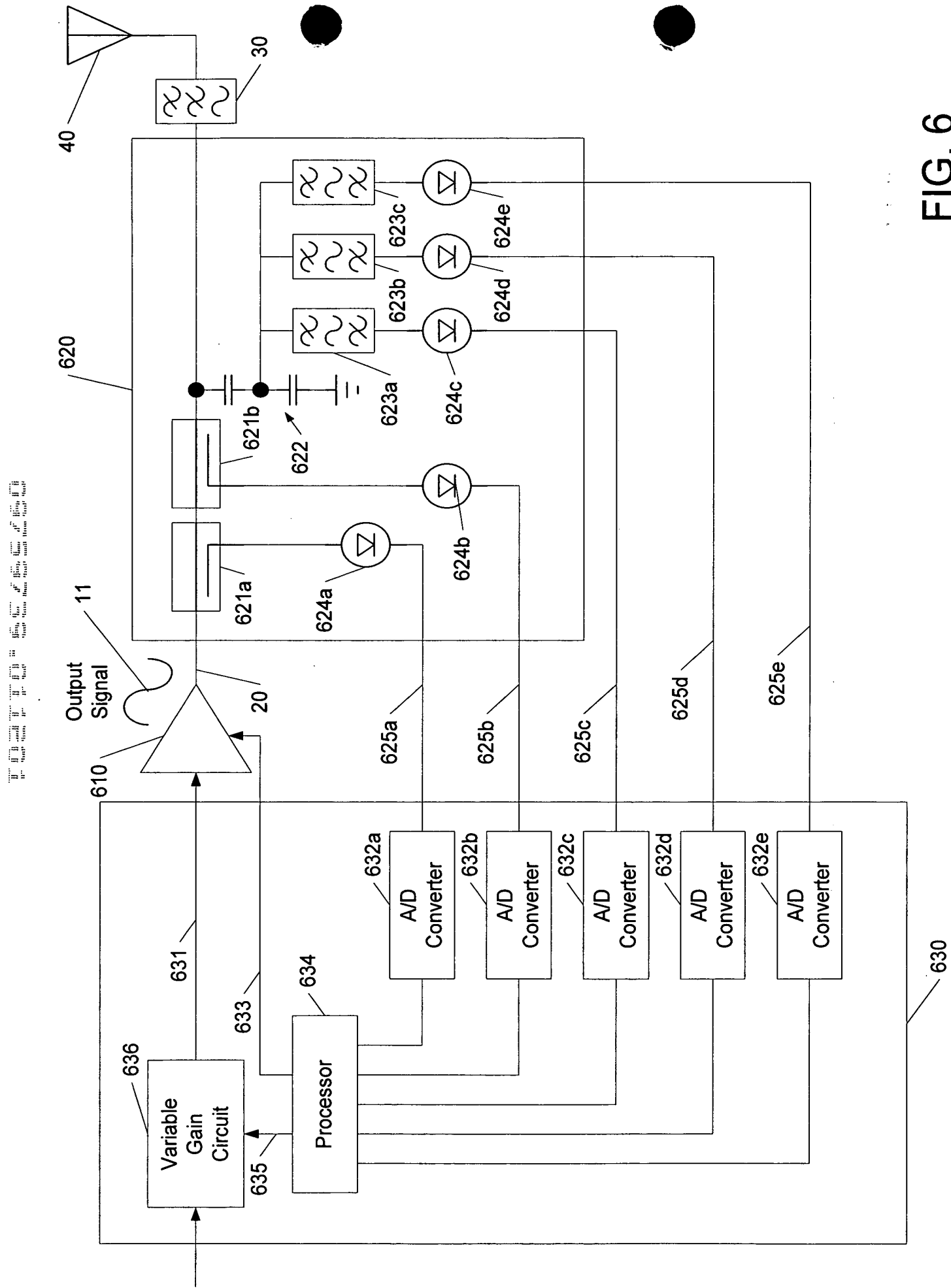


FIG. 5



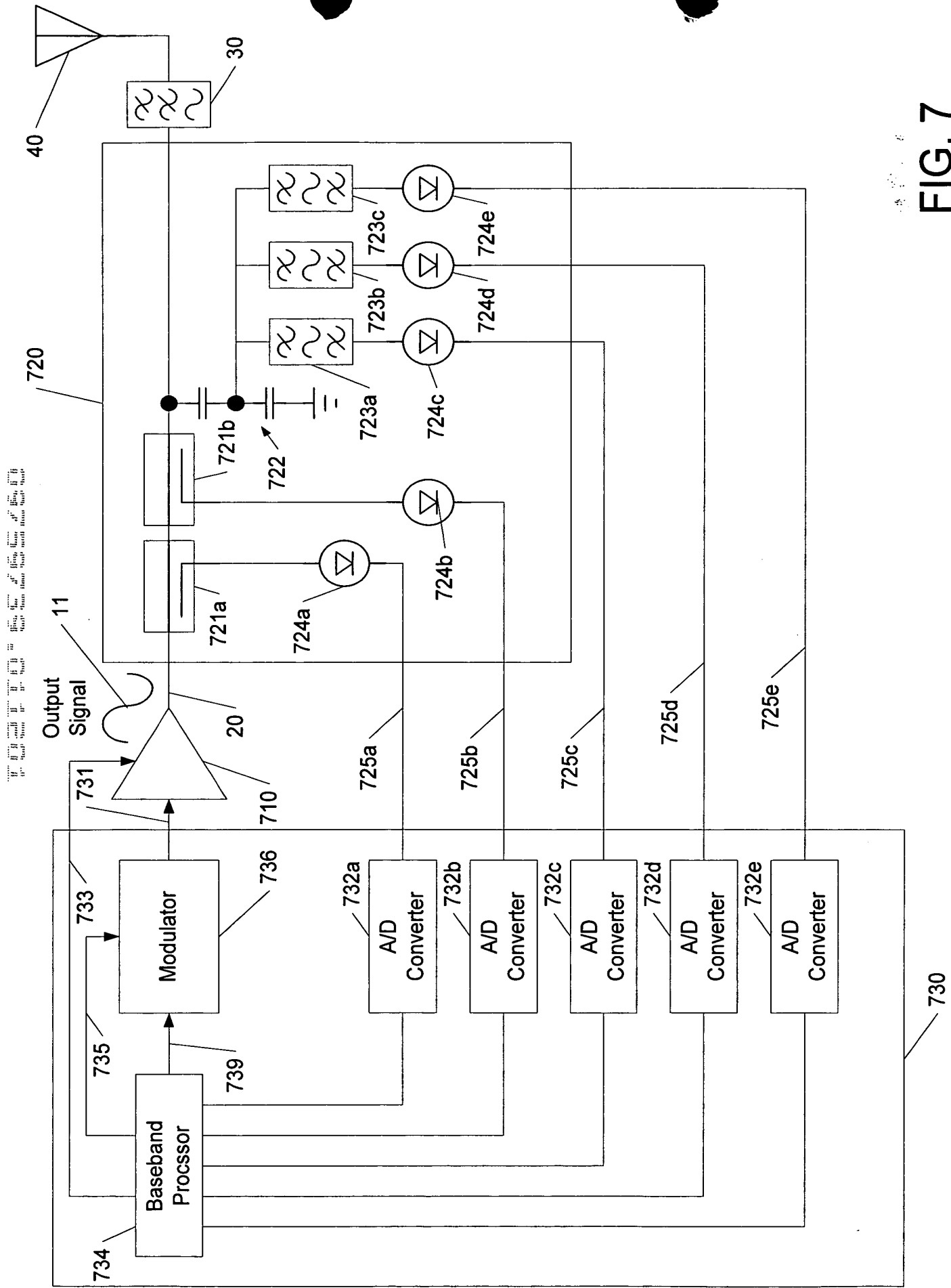


FIG. 7

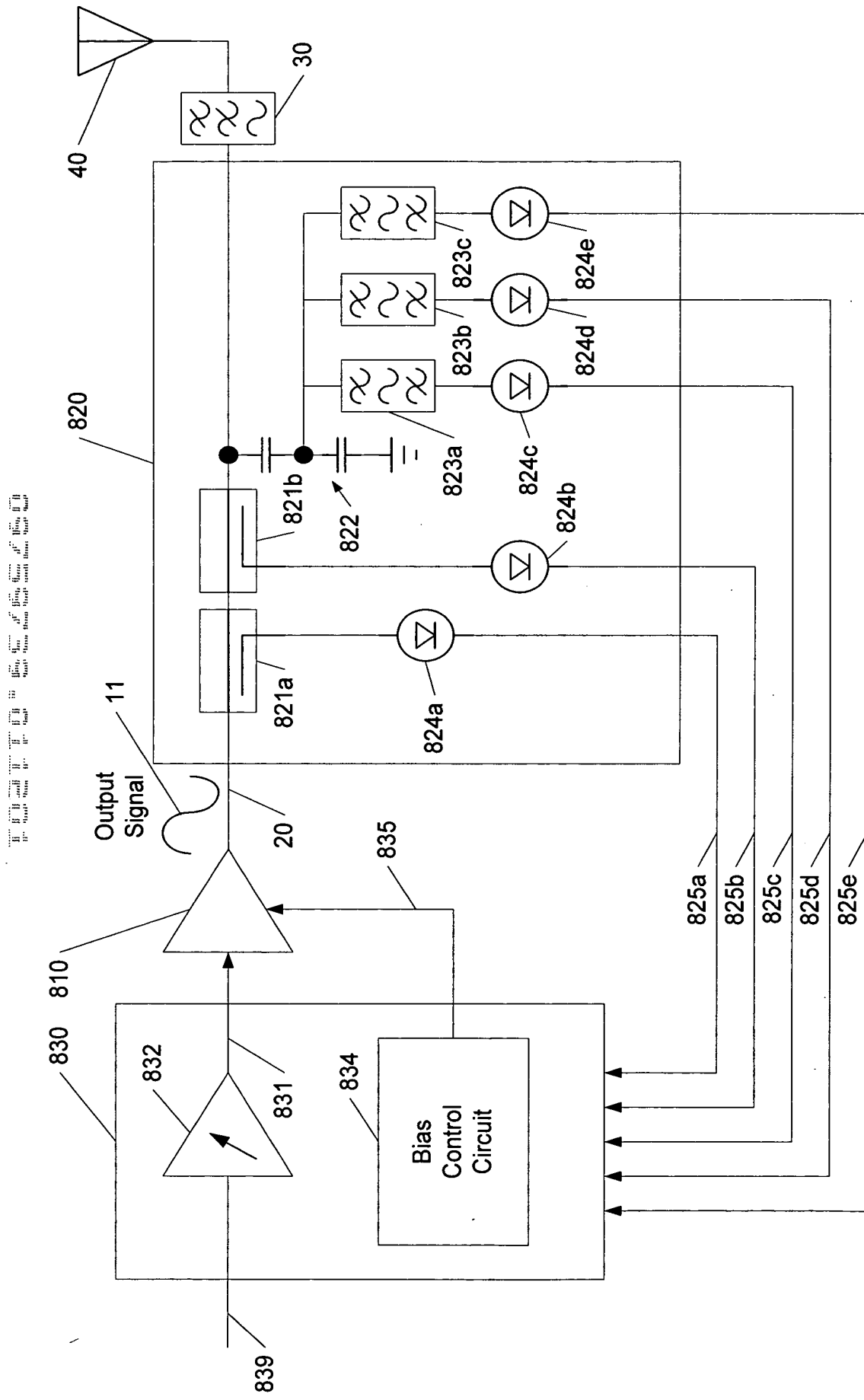


FIG. 8



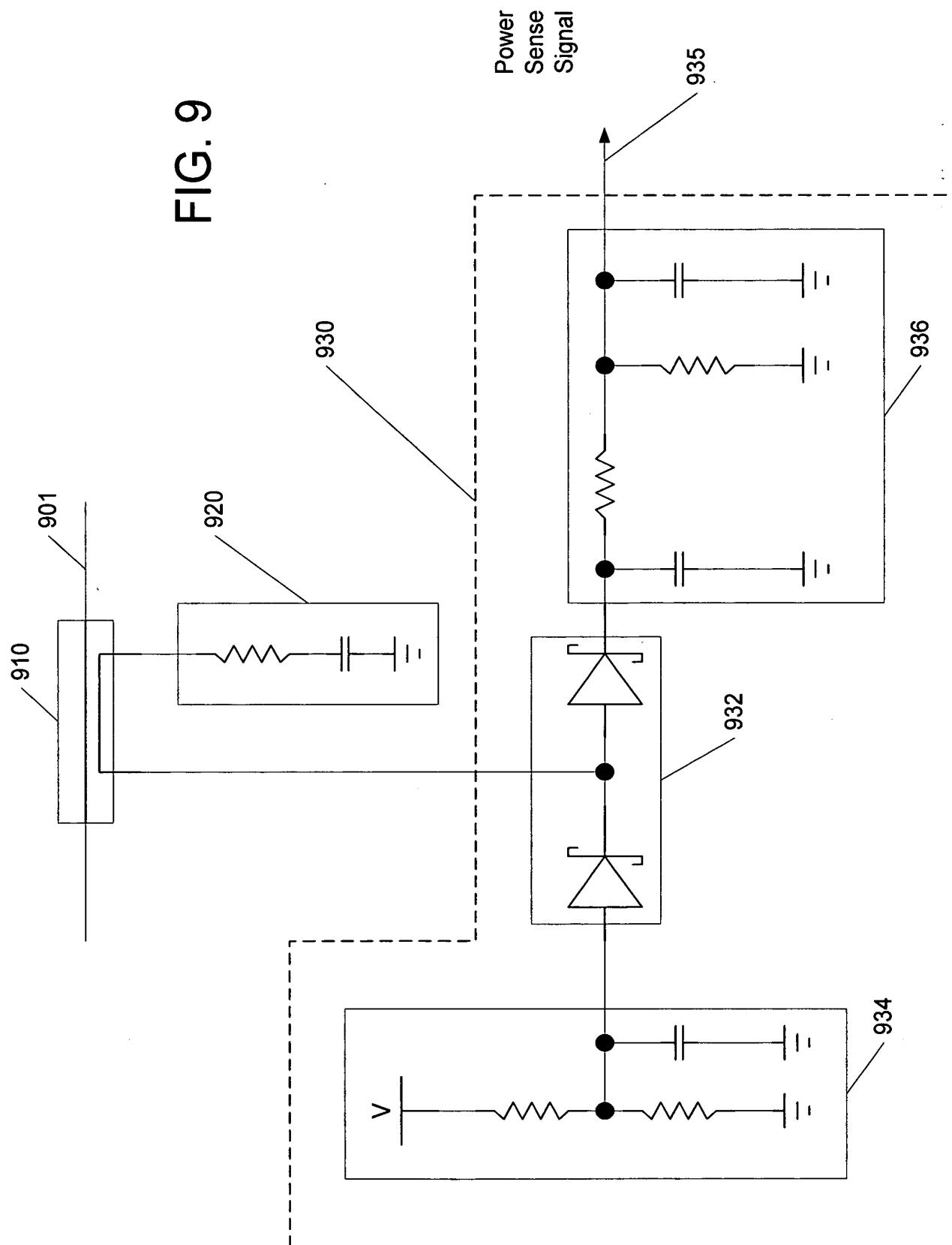


FIG. 10 is a block diagram of a power sense signal processing circuit 1000. The circuit 1000 includes a first threshold detector circuit 1010a, a second threshold detector circuit 1010b, a first comparator 1020a, a second comparator 1020b, and a third comparator 1030. The first threshold detector circuit 1010a receives a power sense signal (fundamental) 1001a and outputs a signal to the first comparator 1020a. The second threshold detector circuit 1010b receives a power sense signal (harmonic) 1001b and outputs a signal to the second comparator 1020b. The first comparator 1020a compares the output of the first threshold detector circuit 1010a with a first threshold value and outputs a signal to the third comparator 1030. The second comparator 1020b compares the output of the second threshold detector circuit 1010b with a second threshold value and outputs a signal to the third comparator 1030. The third comparator 1030 compares the outputs of the first and second comparators 1020a and 1020b and outputs a comparison signal 1005.

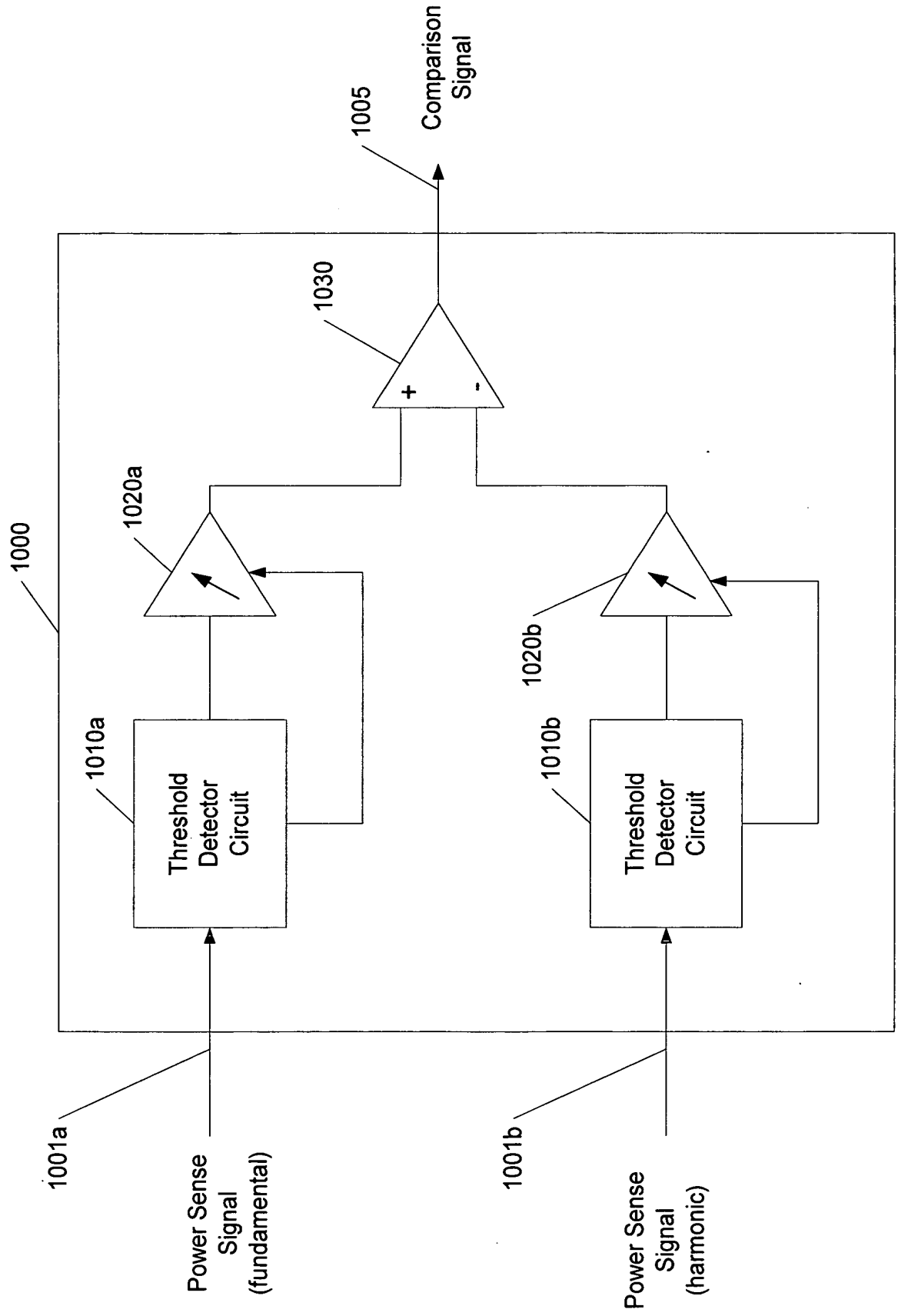


FIG. 10